REMARKS

Introduction

Claims 1-11 remain in the application, of which claims 1 and 11 are in independent form.

Rejections under 35 U.S.C. § 102(b)

Claims 1, 3, 4 and 9-11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,933,846 (*Humphrey*).

Claim 1 of the present application recites, *inter alia*, a "data processing apparatus" that includes "a detection unit … arranged to detect repetitions of a period of an address pattern" and "a state holding element … having an input coupled to the detection unit … to switch the first and second selectable connections in response to the detection of a new one of said repetitions, so that identical addresses from the data processing units (10a,b) alternately map to different ones of the memory units (18a,b) during successive repetitions."

A feature that is novel about the invention recited by claim 1 of the present application (and that is clearly recited in the claim language of claim 1) is that "a detection unit … detect[s] **repetitions of a period of an address pattern**," such that "first and second selectable connections" are switched **"in response to the detection of a new one of said repetitions**." Thus, "**identical addresses** from the data processing units (10a,b) alternately **map to different ones of the memory units** (18a,b) **during successive repetitions**."

Thus, with the apparatus as recited by claim 1 of the present application, repetition of the identical address will trigger mapping to a different memory unit.

As understood by applicants, *Humphrey* describes a system where memory is selected based on a 4-bit code that is included as part of the data stream. As described by *Humphrey*:

> [t]he output of latch 262 is the 24-bit Bank 0 address field. This is split into three buses, namely, bus 274 which contains bits 2-17 of the address field and forms the 16-bit address for the Bank 0 RAM memory 298; bus 276 which is comprised of bits 18 and 19 which provide inputs to the chip select decoder 284; and, finally, bus 278, which is comprised of bits 20-23 and which provide an input to comparator 280. The other input to comparator 280 is from address range circuitry 266. **The address range is a 4-bit code which is uniquely hard-wired for each of the 16 possible slots that a memory array board may be connected to. If the address range identified by circuitry 266 is equal to the upper four bits of the address field, the requested address is within the assigned address range of the memory array board**. Thus, the output of comparator 280 enables the output of decode circuitry 284, via line 283, to generate one of four possible chip selects on chip select bus 285.

(*Humphrey* at col. 10, ln. 58, to col. 11, ln. 7) (emphasis added).

Humphrey does not describe detecting "repetitions in the pattern of addresses supplied by the processing unit," and "[u]pon detection of a repetition the switching unit switch[ing] the selection of the memory unit that is connected to the data processing unit," as recited by claim 1 of the present application. In stark contrast, *Humphrey* describes selecting a memory array board based on a 4-bit code that is included in the data stream. With the apparatus described by *Humphrey*, repetition of the same address (4-bit code) will direct the stream to the same memory array board. *Humphrey* does not, "[u]pon detection of a repetition the switching unit [switch] the selection of the memory unit that is connected to the data processing unit," as recited by claim 1 of the present application.

Thus, in the system described by *Humphrey,* repetition of the same address (4-bit code) will direct the stream to the same memory array board. In stark contrast, with the

apparatus as recited by claim 1 of the present application, repetition of the identical address will trigger mapping to a different memory unit.

Accordingly, for at least these reasons, claim 1 is deemed to distinguish patentably over *Humphrey*.

Claims 3, 4, 9 and 10 depend from, and further define the invention of claim 1, that has been discussed above and is believed to be allowable over *Humphrey*. Accordingly, for at least these reasons, claim 3, 4, 9 and 10 are deemed to distinguish patentably over *Humphrey*.

Independent claim 11, while different in scope than claim 1, recites a method having many of the features described above with respect to claim 1. For example, claim 11 recites "detecting repetition of periods of access address patterns output from at least one of a plurality of processing units" and "switching selectable connections … so that a same addresses from at least one of the plurality of processing units alternately addresses a location in different ones of the memory units in dependence on the detection of said repetition," which features, as described above, are not taught or suggested by *Humphrey*.

Accordingly, for at least these reasons, claim 11 is deemed to distinguish patentably over *Humphrey*.

Rejections under 35 U.S.C. § 103(a)

Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Humphrey* in view of U.S. Patent No. 4,939,636 (*Nakagawa*).

Claim 2 depends from, and further defines the invention of claim 1, that has been discussed above and is believed to be allowable over *Humphrey*.

Nakagawa is directed to a memory management system, but does not make up for the deficiencies of *Humphrey*. Accordingly, for at least these reasons, claim 2 is deemed to distinguish patentably over any hypothetical *Humphrey-Nakagawa* combination.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Humphrey* in view of U.S. Patent No. 4,583,163 (*Kobayashi*).

Claim 5 depends from, and further defines the invention of claim 1, that has been discussed above and is believed to be allowable over *Humphrey*.

Kobayashi is directed to a data prefetch apparatus, but does make up for the deficiencies of *Humphrey*.

Accordingly, for at least these reasons, claim 5 is deemed to distinguish patentably over any hypothetical *Humphrey- Kobayashi* combination.

Claims 6-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Humphrey* in view of U.S. Patent No. 5,673,383 (*Sukegawa*).

Claims 6-8 depend from, and further define the invention of claim 1, that has been discussed above and is believed to be allowable over *Humphrey*.

Sukegawa is directed to flash memory storage system, but does make up for the deficiencies of *Humphrey*.

Accordingly, for at least these reasons, claims 6-8 are deemed to distinguish patentably over any hypothetical *Humphrey-Sukegawa* combination.

Thus, applicants submit that each of the claims of the present application are patentable over each of the references of record, either taken alone, or in any proposed hypothetical combination. Accordingly, withdrawal of the rejections to the claims is respectfully requested.

Conclusion

In view of the above remarks, reconsideration and allowance of the present application is respectfully requested.

Respectfully submitted,

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